CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor component, comprising:

forming a first patterned device layer having a first predetermined etch removal time on a portion of a common layer;

forming a second device layer having a second predetermined etch removal time on an adjacent portion of the common layer, the second predetermined etch removal time being greater than the first predetermined etch removal time;

forming a patterned sacrificial layer onto the first patterned device layer, the sacrificial layer having a third predetermined etch removal time;

forming a first hard mask on a portion of the patterned sacrificial layer defining a first exposed patterned portion, and forming a second hard mask on a portion of the second device layer defining a second exposed patterned portion; and

etching the first exposed patterned portion and the second exposed patterned portion substantially simultaneously to the common layer defining a first stack comprising the first hard mask, a device-sized sacrificial layer, and a first device, and defining a second stack comprising the second hard mask and a second device.

2. The method of claim 1, further comprising:

predetermining the first predetermined etch removal time by calculating the ratio of a first device layer thickness and a first device layer etch rate, and predetermining the second predetermined etch removal time by calculating the ratio of a second device layer thickness and a second device layer etch rate, calculating an etch removal time differential by subtracting the first from the second etch removal times, and wherein forming a sacrificial layer onto the first device layer comprises determining a sacrificial layer thickness as the product of the etch removal time differential and a sacrificial layer etch rate, and forming the sacrificial layer onto the first device layer to the sacrificial layer thickness.

3. The method of claim 1, further comprising:

removing the first hard mask and device-sized sacrificial layer exposing the first device, and removing the second mask exposing the second device; and

passivating and planarizing the first and second devices with an encasing passivation layer.

4. The method of claim 1, further comprising;

removing the first hard mask and device-sized sacrificial layer exposing the first device, and removing the second mask exposing the second device;

depositing a conformal passivation layer on the common layer and first and second devices; and

encasing and planarizing the first and second devices with an encasing passivation layer.

5. The method of claim 1 further comprising:

providing an encasing passivation layer on the common layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing the first hard mask;

removing the first hard mask and the device-sized sacrificial layer exposing the first device and defining a first cavity;

lowering the elevation of the passivation layer surface to expose the second hard mask; and

removing the second hard mask exposing a second device and defining a second cavity.

6. The method of claim 1, wherein forming a sacrificial layer onto the first device layer comprises:

depositing a conformal passivation layer on the common layer and first and second device stacks;

providing an encasing passivation layer on the conformal passivation layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing a first portion of the conforming passivation layer;

removing the first portion of the conforming passivation layer, first hard mask and the device-sized sacrificial layer exposing the first device and defining a first cavity with a passivation liner;

lowering the elevation of the passivation layer surface to exposing a second portion of the conforming passivation layer; and

removing the second portion of the conforming passivation layer and the second hard mask exposing a second device and defining a second cavity with a passivation liner.

7. The method of claim 1, wherein forming a patterned sacrificial layer onto the first patterned device layer, the sacrificial layer having a third predetermined etch removal time comprises forming a patterned etch stop layer onto the first patterned device layer and forming a patterned sacrificial layer onto the patterned etch stop layer, the sacrificial layer and the etch stop layer having a combined third predetermined etch removal time.

8. The method of claim 1, wherein etching the first and second exposed patterned portion comprises:

etching the first and second exposed patterned portion using a wet etch process.

9. The method of claim 5, wherein lowering the elevation of the passivation layer surface comprises:

etching the encasing passivation layer using a dry etch process layer.

10. The method of claim 1, wherein forming a first and second hard mask comprises forming a first and second hard mask comprising a material selected from the group consisting of silicon dioxide, silicon nitride, and metal.

11. A method for fabricating microelectronic components, comprising:

forming a first device layer on at least a portion of a common layer, an etch stop layer on the first device layer, and a sacrificial layer on the etch stop layer, the first device layer having a first predetermined etch removal time, the etch stop layer having a predetermined etch stop etch removal time, and the sacrificial layer having a predetermined sacrificial layer etch removal time;

forming a mask on at least a portion of the sacrificial layer, the mask defining a first exposed portion adjacent the mask;

removing the first exposed portion defining a patterned sacrificial layer, patterned etch stop layer, and a patterned first device layer, and an exposed common layer portion;

removing the mask;

forming a second device layer on at least a portion of the exposed common layer portion adjacent the patterned first device layer, the second device layer having a second predetermined etch removal time substantially equal to the sum of the predetermined first device etch removal time, predetermined etch stop etch removal time and the predetermined sacrificial layer etch removal time;

forming a first hard mask on a portion of the patterned sacrificial layer defining a first exposed patterned portion, and forming a second hard mask on a portion of the second device layer defining a second exposed patterned portion; and

etching the first exposed patterned portion and the second exposed patterned portion substantially simultaneously to the common layer defining a first stack

comprising the first hard mask, a device-sized sacrificial layer, a device-sized etch stop layer, and a first device, and defining a second stack comprising the second hard mask and a second device.

12. The method of claim 11, further comprising:

predetermining the first predetermined etch removal time by calculating the ratio of a first device layer thickness and a first device layer etch rate, and predetermining the second predetermined etch removal time by calculating the ratio of a second device layer thickness and a second device layer etch rate, calculating an etch removal time differential by subtracting the first from the second etch removal times, and wherein forming a sacrificial layer onto the first device layer comprises determining a sacrificial layer thickness as the product of the etch removal time differential and a sacrificial layer etch rate, and forming the sacrificial layer onto the first device layer to the sacrificial layer thickness.

13. The method of claim 11 further comprising:

removing the first hard mask, device-sized sacrificial layer, and device-sized etch stop layer exposing the first device, and removing the second mask exposing the second device; and

passivating and planarizing the first and second devices with an encasing passivation layer.

14. The method of claim 11, further comprising:

removing the first hard mask, device-sized sacrificial layer, and device-sized etch stop layer exposing the first device, and removing the second mask exposing the second device;

depositing a conformal passivation layer on the common layer and first and second devices; and

encasing and planarizing the first and second devices with an encasing passivation layer.

15. The method of claim 11, further comprising:

providing an encasing passivation layer on the common layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing the first hard mask;

removing the first hard mask, the device-sized sacrificial layer, and the device-sized etch stop layer exposing the first device and defining a first cavity;

lowering the elevation of the passivation layer surface to expose the second hard mask; and

removing the second hard mask exposing a second device and defining a second cavity.

16. The method of claim 11, further comprising:

depositing a conformal passivation layer on the common layer and first and second device stacks;

providing an encasing passivation layer on the conformal passivation layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing a first portion of the conforming passivation layer;

removing the first portion of the conforming passivation layer, first hard mask, the device-sized sacrificial layer and the etch stop layer exposing the first device and defining a first cavity with a passivation liner;

lowering the elevation of the passivation layer surface to exposing a second portion of the conforming passivation layer; and

removing the second portion of the conforming passivation layer and the second hard mask exposing a second device and defining a second cavity with a passivation liner.

17. The method of claim 11, wherein etching the first and second exposed patterned portion comprises:

etching the first and second exposed patterned portion using a wet etch process.

18. The method of claim 16, wherein lowering the elevation of the passivation layer surface comprises:

etching the passivation layer using a dry etch process layer.

19. The method of claim 11, wherein forming a first and second hard mask layer comprises forming a first and second hard mask layer comprising a material selected from the group consisting of silicon dioxide, silicon nitride, and metal.

20. A method for fabricating an assembly, comprising:

interconnecting a plurality of components wherein at least one comprises a device, the device fabricated using a method comprising:

forming a first patterned device layer having a first predetermined etch removal time on a portion of a common layer;

forming a second device layer having a second predetermined etch removal time on an adjacent portion of the common layer, the second predetermined etch removal time being greater than the first predetermined etch removal time;

forming a patterned sacrificial layer onto the first patterned device layer, the sacrificial layer having a third predetermined etch removal time;

forming a first hard mask on a portion of the patterned sacrificial layer defining a first exposed patterned portion, and forming a second hard mask on a portion of the second device layer defining a second exposed patterned portion; and

etching the first exposed patterned portion and the second exposed patterned portion substantially simultaneously to the common layer defining a first stack comprising the first hard mask, a device-sized sacrificial layer, and a first device, and defining a second stack comprising the second hard mask and a second device.

21. The method of claim 20, further comprising:

predetermining the first predetermined etch removal time by calculating the ratio of a first device layer thickness and a first device layer etch rate, and predetermining the second predetermined etch removal time by calculating the ratio of a second device layer thickness and a second device layer etch rate, calculating an etch removal time differential by subtracting the first from the second etch removal times, and wherein forming a sacrificial layer onto the first device layer comprises determining a sacrificial layer thickness as the product of the etch removal time differential and a sacrificial layer etch rate, and forming the sacrificial layer onto the first device layer to the sacrificial layer thickness.

22. The method of claim 20, further comprising:

removing the first hard mask and device-sized sacrificial layer exposing the first device, and removing the second mask exposing the second device; and

passivating and planarizing the first and second devices with an encasing passivation layer.

23 The method of claim 20 further comprising;

removing the first hard mask and device-sized sacrificial layer exposing the first device, and removing the second mask exposing the second device;

depositing a conformal passivation layer on the common layer and first and second devices; and

encasing and planarizing the first and second devices with an encasing passivation layer.

24. The method of claim 20 further comprising:

providing an encasing passivation layer on the common layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing the first hard mask;

removing the first hard mask and the device-sized sacrificial layer exposing the first device and defining a first cavity;

lowering the elevation of the passivation layer surface to expose the second hard mask; and

removing the second hard mask exposing a second device and defining a second cavity.

25. The method of claim 20, wherein forming a sacrificial layer onto the first device layer comprises:

depositing a conformal passivation layer on the common layer and first and second device stacks;

providing an encasing passivation layer on the conformal passivation layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks;

lowering the elevation of the passivation layer surface exposing a first portion of the conforming passivation layer;

removing the first portion of the conforming passivation layer, first hard mask and the device-sized sacrificial layer exposing the first device and defining a first cavity with a passivation liner;

lowering the elevation of the passivation layer surface to exposing a second portion of the conforming passivation layer; and

removing the second portion of the conforming passivation layer and the second hard mask exposing a second device and defining a second cavity with a passivation liner.

26. The method of claim 20, wherein forming a patterned sacrificial layer onto the first patterned device layer, the sacrificial layer having a third predetermined etch removal time comprises forming a patterned etch stop layer onto the first patterned device layer and forming a patterned sacrificial layer onto the patterned etch stop layer, the sacrificial layer and the etch stop layer having a combined third predetermined etch removal time.

27. The method of claim 20, wherein etching the first and second exposed patterned portion comprises:

etching the first and second exposed patterned portion using a wet etch process.

28. The method of claim 24, wherein lowering the elevation of the passivation layer surface comprises:

etching the encasing passivation layer using a dry etch process layer.

29. The method of claim 20, wherein forming a first and second hard mask comprises forming a first and second hard mask comprising a material selected from the group consisting of silicon dioxide, silicon nitride, and metal.